

FIG. 1

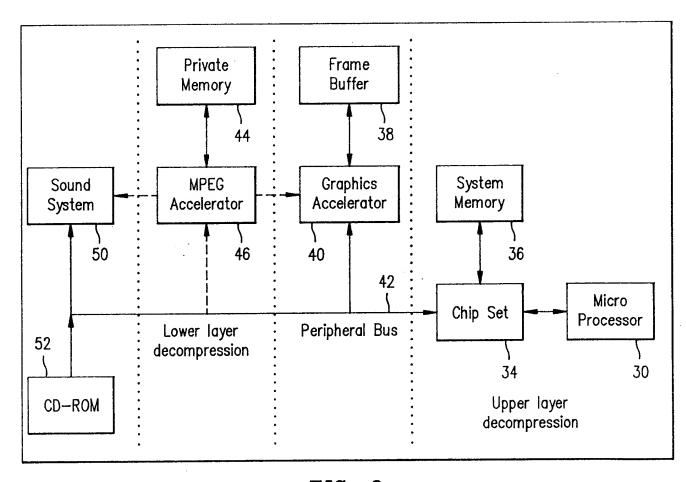


FIG. 2

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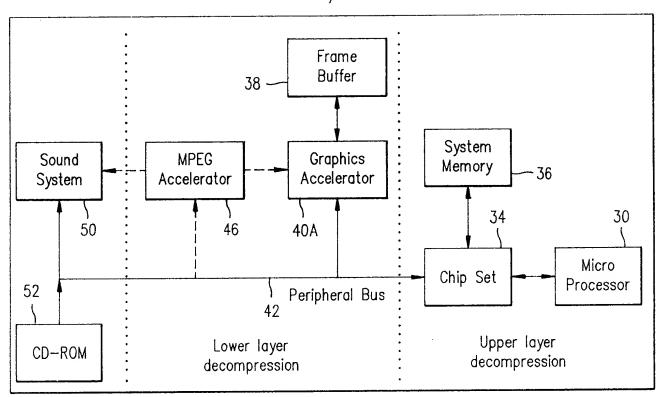


FIG. 3

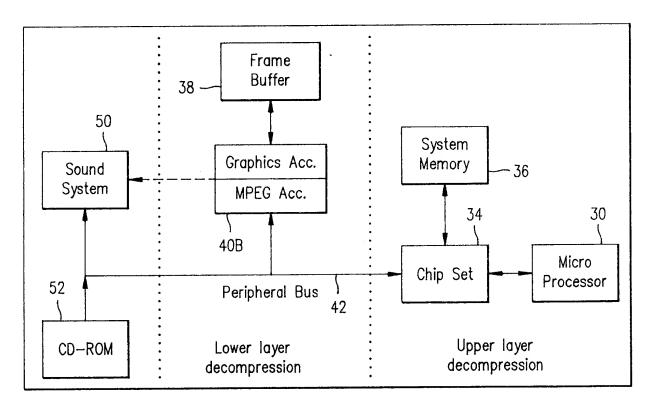


FIG. 4

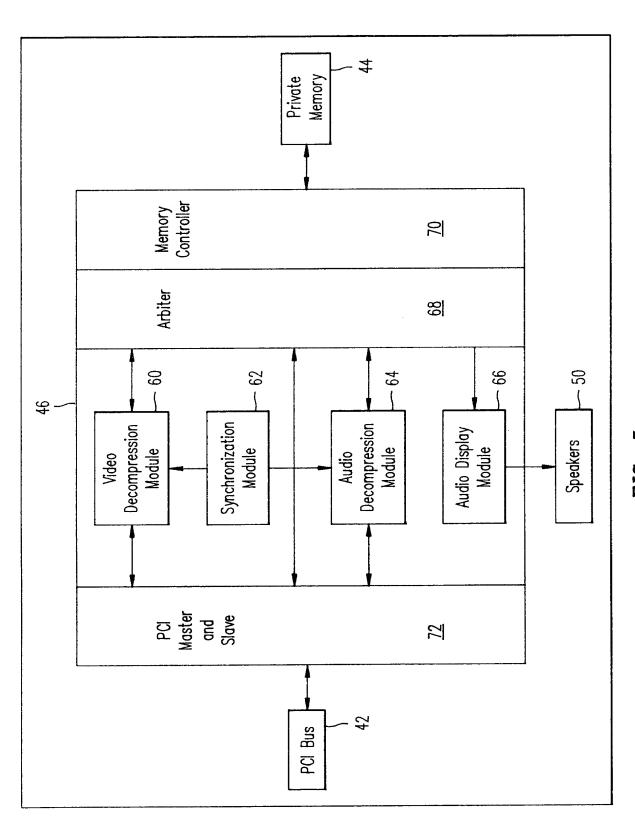


FIG. 5

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Sto Fra						Start rame
Display			display IO frame	display B1 frame	display B2 frame	display P3 frame
VDE	decode IO frame	decode P3 frame	decode B1 frame	decode B2 frame	decode P6 frame	decode 84 frame
Host (Software) Driver	P3 Program	B1 Program	B2 Program	P6 Program	B4 Program	B5 Program

FIG. 6

Sto Fra						art Ime
Display			display IO frame	no display B1 frame	display B2 frame	display P3 frame
VDE	decode IO frame	decode P3 frame	decode B1 frame abandon B1 frame	decode B2 frame	decode P6 frame	decode B4 frame
Host (Software) Driver	P3 Program	B1 Program	B2 Program	P6 Program	B4 Program	

FIG. 7

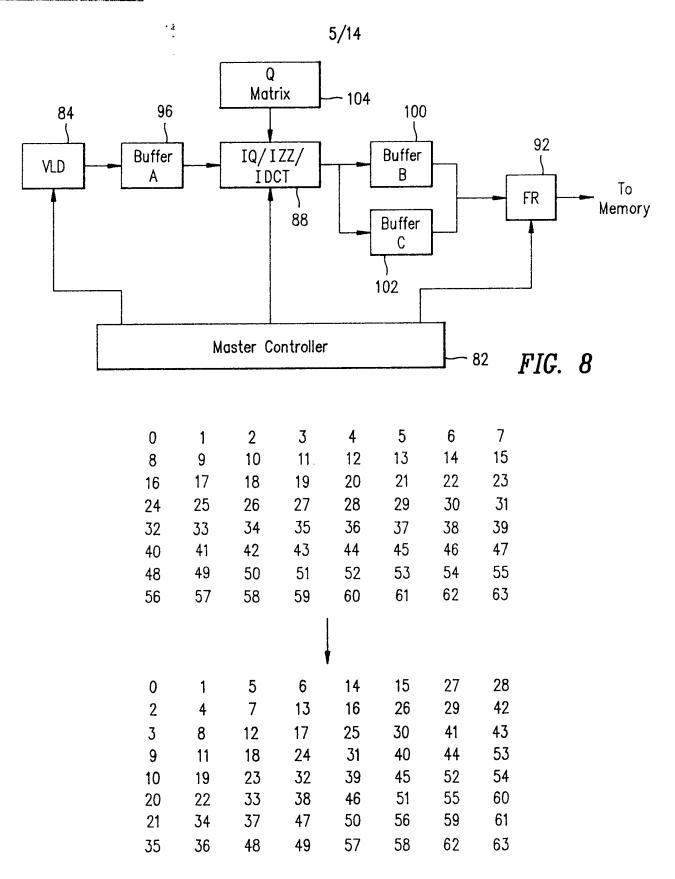


FIG. 9

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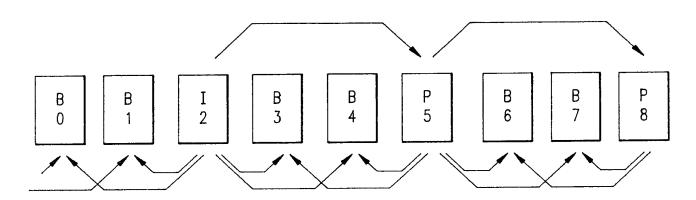
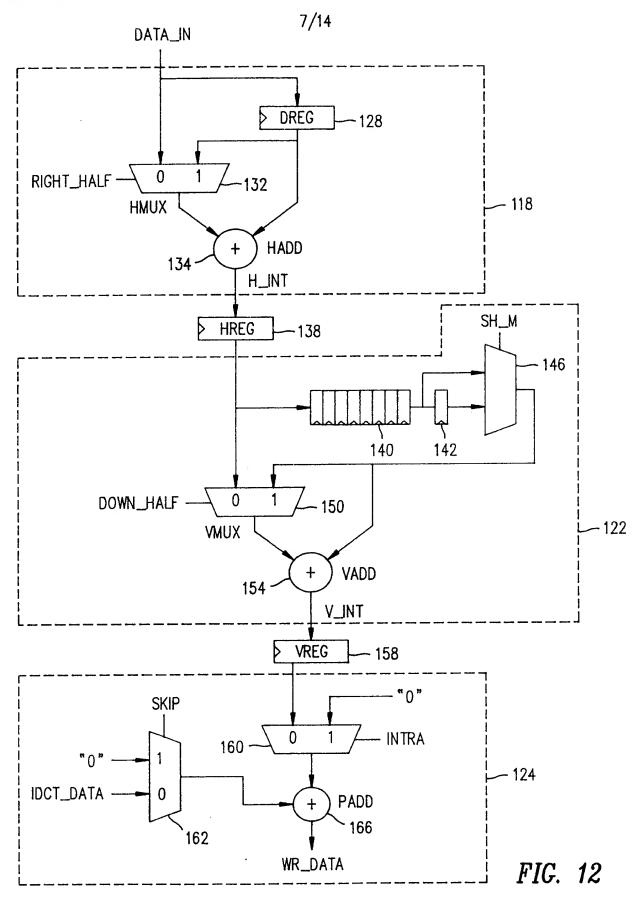


FIG. 10

1 begin			
		end 1 2 begin	
end 2	3 begin	end 3 4 begin)
·			
		end 4 5 begin	
			end 5
6 begin			
		end 6 7 begir	1
end 7 8	8 9 begin	end 9 10 begin	
			end 10

FIG. 11



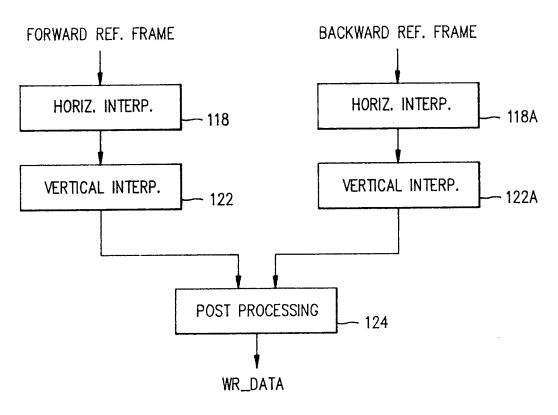
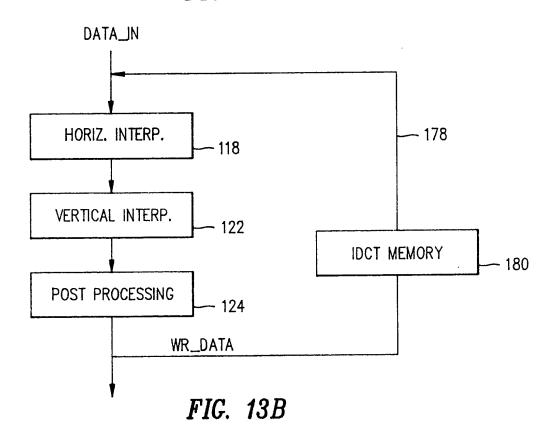


FIG. 13A



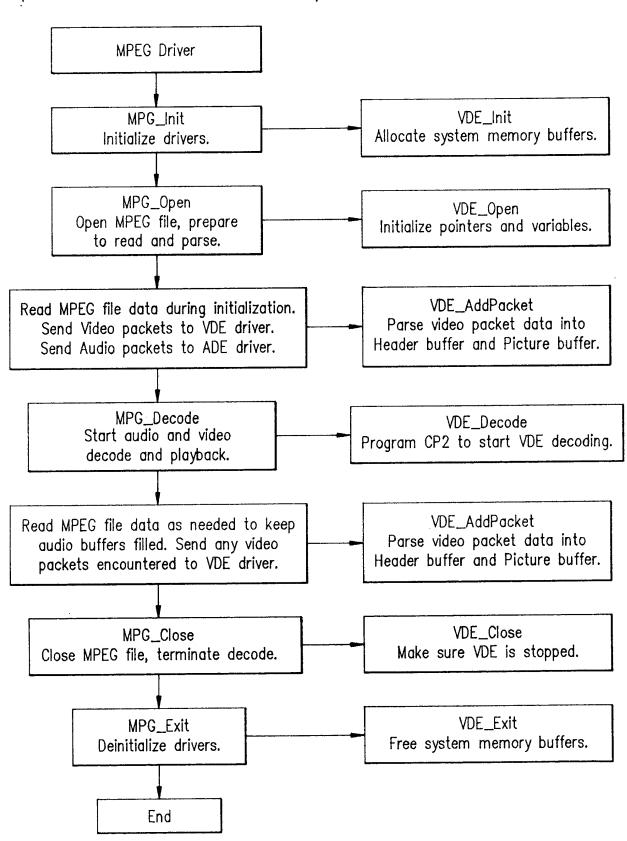


FIG. 14A

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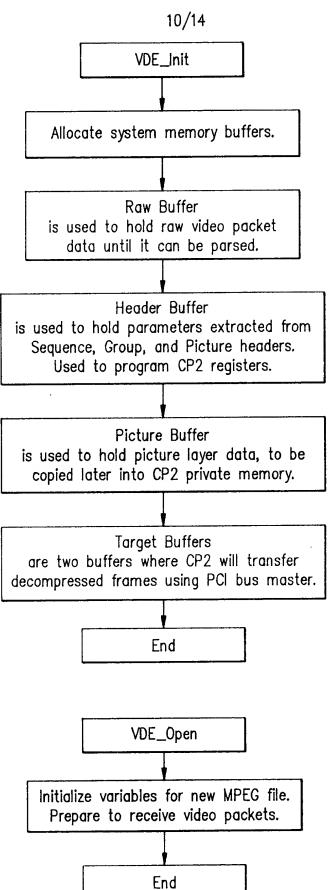
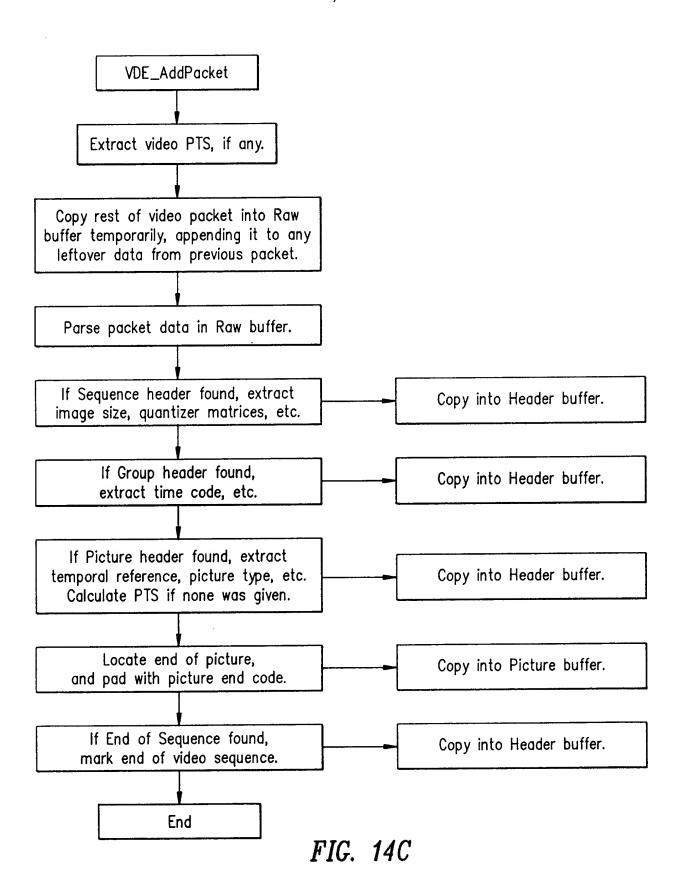


FIG. 14B



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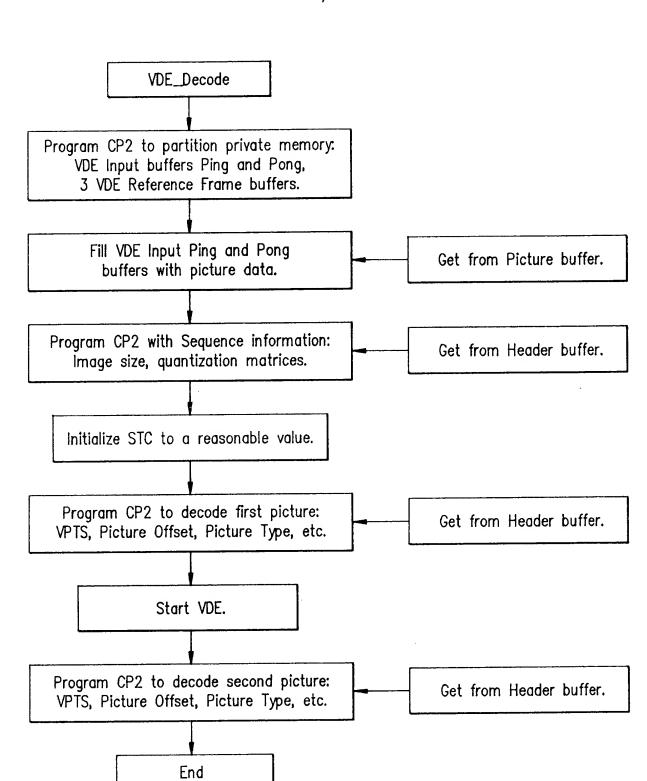


FIG. 14D

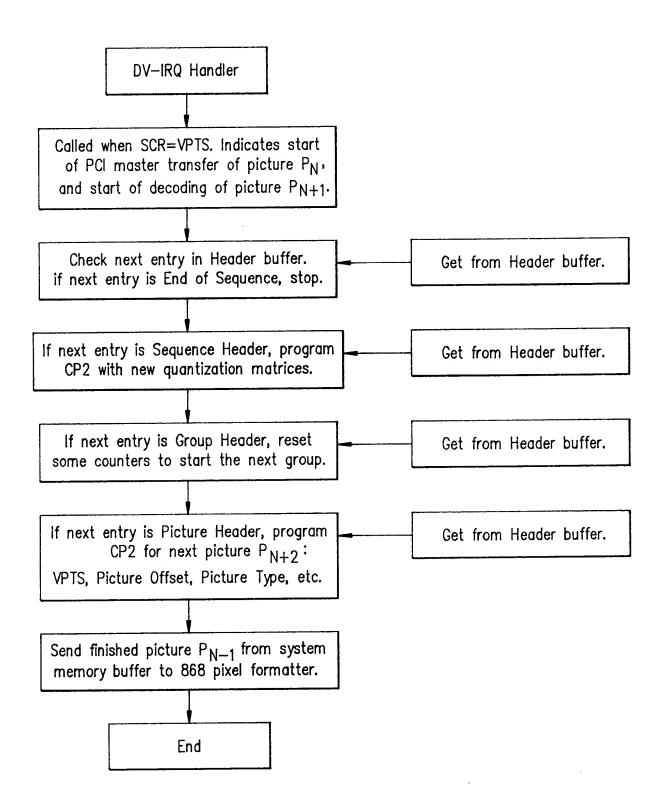


FIG. 14E

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